PAL is clocked by Clk40H (rising edge).
All outputs are determined purely by state, not by transitions, except for RCntL.
The TfIP (transfer in progress) signal is generated by the row counter.
Tricky part of timing is insuring that last SC pulse occurs before VRAM row transfer operation, and that first SC pulse of next row occurs sufficiently long after the VRAM transfer operation has completed. Note that SC is delayed different amounts according to direction of Transfer.
Also must be careful that SE is asserted at right times, relative to SC pulses and VRAM row transfer operations.
Whenever TfTrig is asserted, must begin testing for TfEnd immediately, and TfTrig must be de-asserted immediately after TfEnd is detected.
Note that 2049 requests to EMC Communications Register are generated; so Store isn't really over when TfIP goes low.

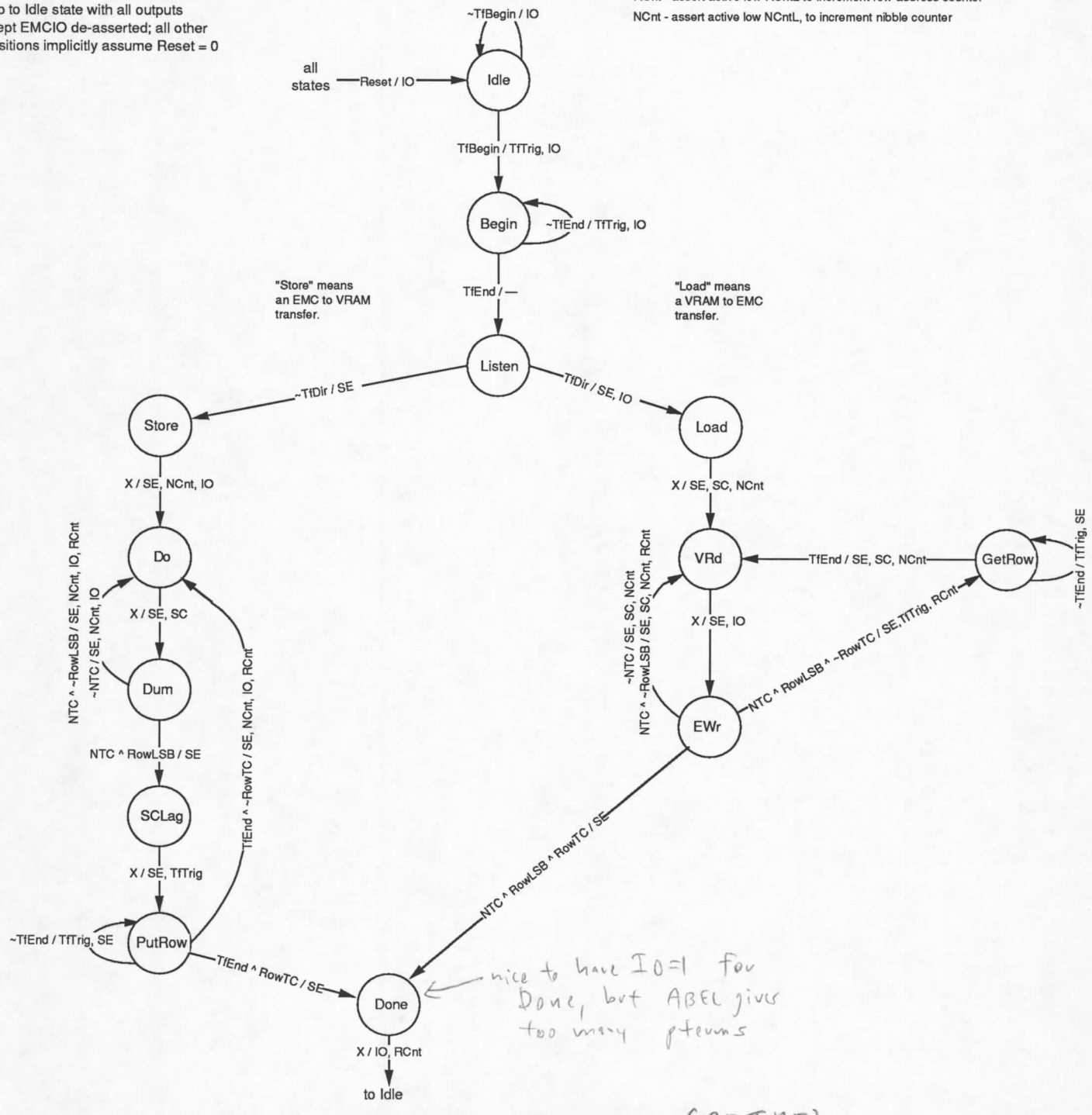
Note: Reset input causes immediate jump to Idle state with all outputs except EMCIO de-asserted; all other transitions implicitly assume Reset = 0

Inputs:

Reset - unconditonally resets to Idle state
TfBegin - (= !TfBeginL) from IGC to initiate a Transfer operation
TfDir - indicates direction of Transfer, 0 for EMC to VRAM ("store"), 1 for VRAM to EMC ("load")
TfEnd - from Backing Store logic, indicates VRAM transfer cycle has completed
NTC - (= !NTCL) indicates nibble counter is at 0
RowLSB - LSB of row counter, acts like MSB of nibble counter
RowTC - (= !RowTCL) row address counter is at 1111

Outputs:

TfTrig - asserts active low TfTrigL to trigger a transfer operation in VRAM control logic
SE - asserts active low SEEnL, which becomes VRAM serial enable signal (SE) after one 20 MHz cycle delay
SC - asserts active low SCEnL, which becomes the VRAM serial clock (SC) after an inverter and a delay which depends on direction of transfer
IO - asserts IOCtl signal to EMCs after one 40 MHz cycle delay
RCnt - assert active low RCntL to increment row address counter
NCnt - assert active low NCntL, to increment nibble counter



nice to have IO=1 for Done, but ABEL gives too many pterms

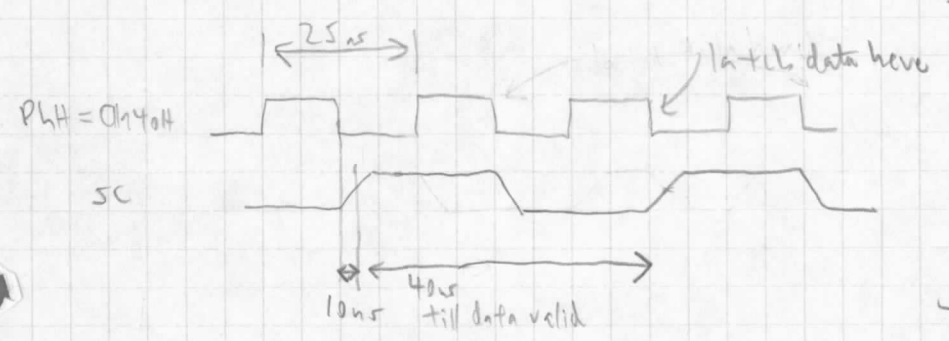
State Diagram for Transfer FSM (RDTRF)

VRAM/EMC Timing 25-Sep-89

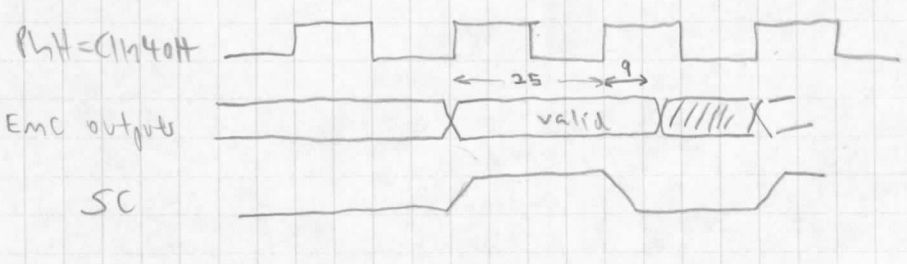
		TI-12	Hitachi -11 or 12
VRAM specs:			
serial-out	SCK↑ to data valid	35	40
	SCK↑ to old data invalid	10	7
serial-in	input setup to SCK↑	3	0
	input hold from SCK↑	5	20

EMC specs

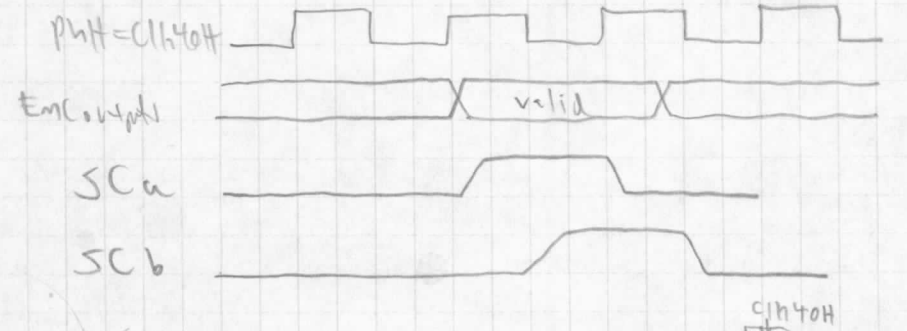
out	PhH↑ to data valid	25
	PhH↑ to old data gone	9
in	input setup to PhH↓	-3
	input hold from PhH↓	9



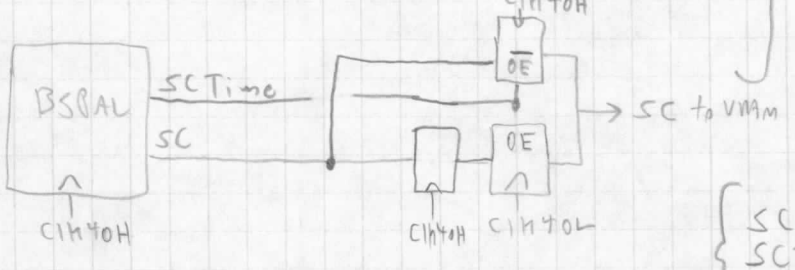
For VRAM → EMC
SC must be -L40F
with 2-13 ns delay



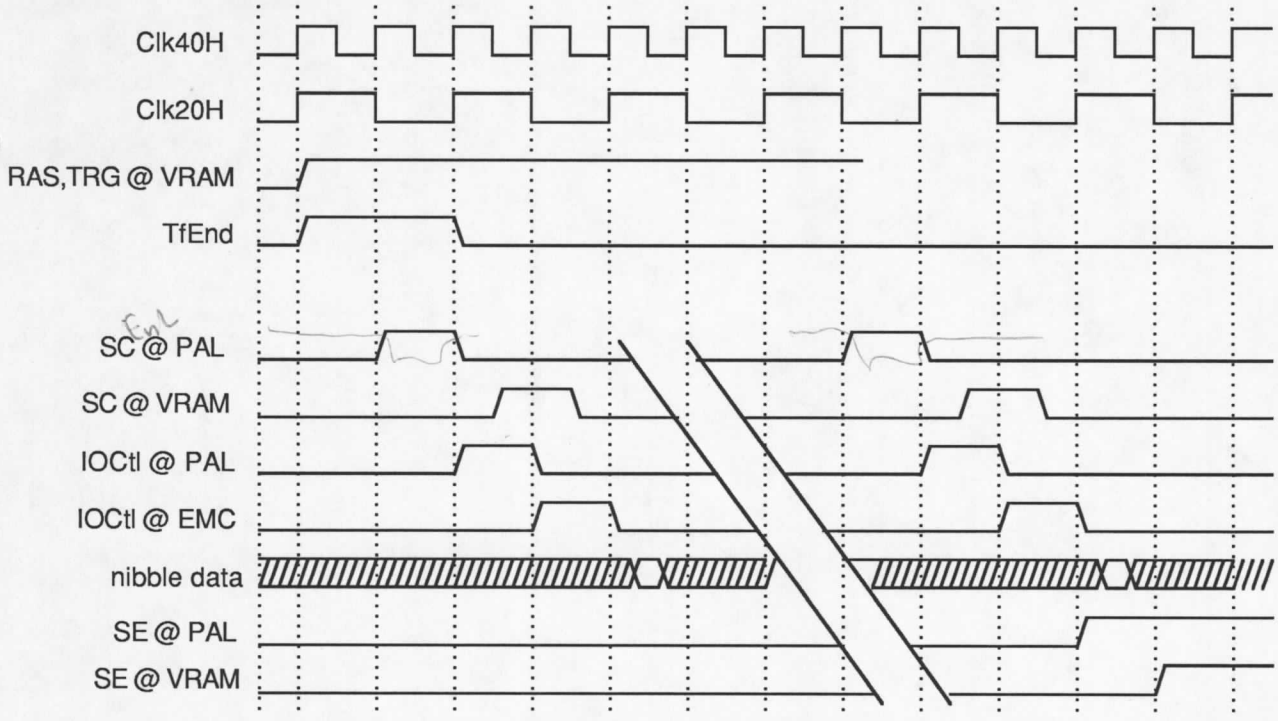
For EMC → Hitachi VRAM
SC must be -L40R
with 0-14 ns delay



For EMC → TI VRAM
SC can be
(a) -L40H w/ 3-29 ns delay
or
(b) -L40F w/ 0-15 ns delay



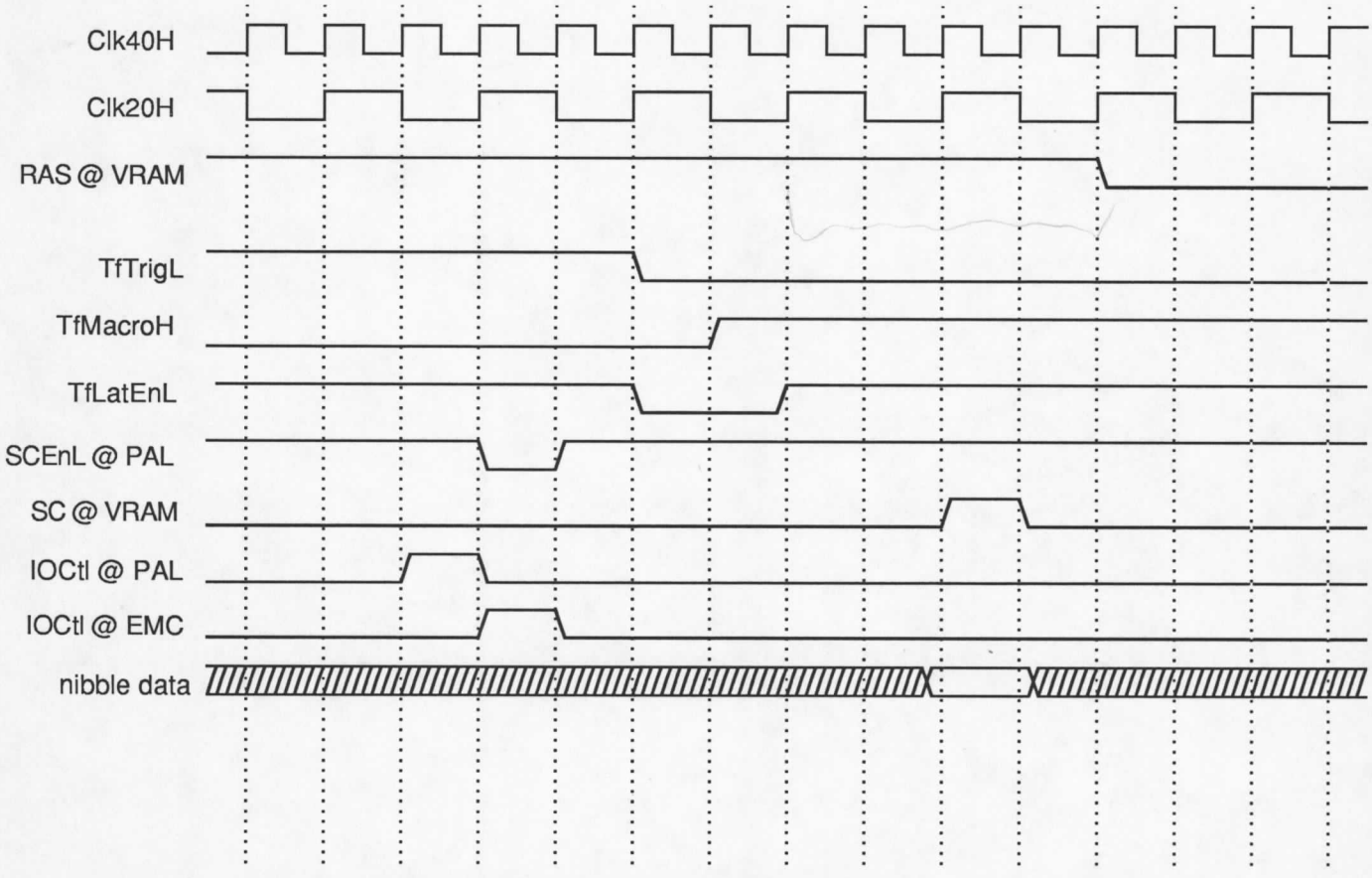
SCTime = 1 For VRAM → EMC
SCTime = 0 For EMC → Hitachi
For EMC → TI



Transfer "Load" Operation (VRAM —> EMC)

Shows first nibble of a row being transferred, then last nibble of the last row.

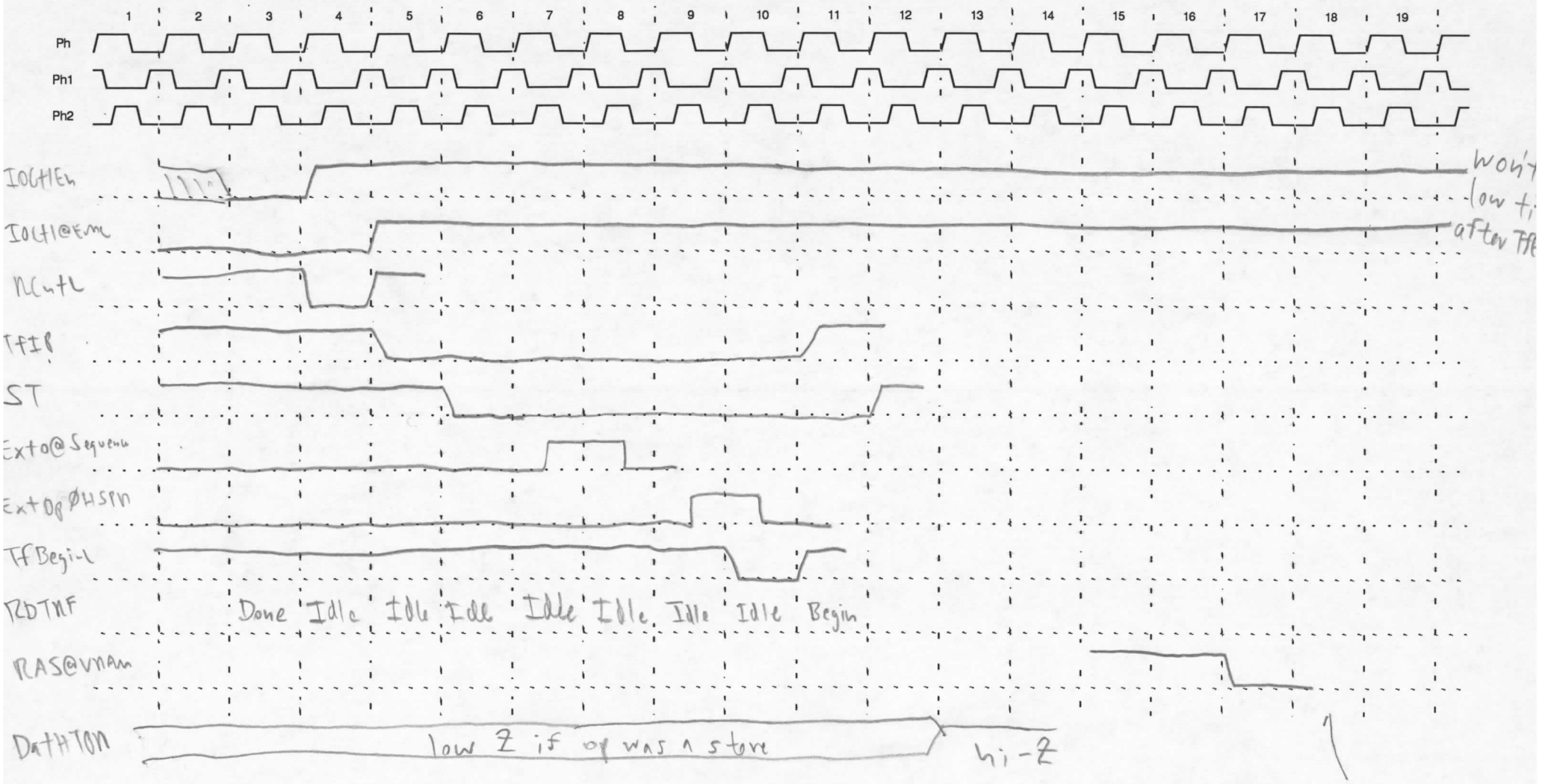
EMC requires data valid from Clk40H falling till 9ns thereafter. VRAM serial out is valid 40 ns after SC rising till 7 ns after next SC rising.



Transfer "Store" Operation (EMC —> VRAM)

Shows last nibble of a row being transferred, followed by quickest possible VRAM transfer operation.

Register Operations End of One Operation & Beginning of Another



(1) need 4 wait cycles between
Ext0pØ asserted to begin a Transfer
and ST2 tested for completion of it

PART TIMINGS FOR TRANSFER OPERATIONS (INCLUDES VRAM TRG CYCLES)

Covers Hitachi -11 parts (Rev 5, Aug 89) and TI -12 parts (April 89)

VRAM PARAMETER	HM534251-11	TMS44C251-12
RAS low to SC hi	?	105
CAS low to SC hi	?	45
RAS hi to SC hi	30	30
TRG hi to SC hi	25	40
old SC hi to RAS low	40	10
D setup before SC (serial-in)	0	3
D hold after SC (serial-in)	20	5
SE setup before SC (serial-in)	0	15
SE hold after SC (serial-in)	35	20

EMC PARAMETER	
data-in setup before Ph low	- 3
data-in hold after Ph low	9
old data-out valid after Ph hi	9
Ph hi to new data-out valid	25